REMARKS

Claims 1-11 are currently pending in the present patent application. In the subject Office Action, the Examiner stated that Fig. 1 should be designated by a legend such as –**Prior Art**--. In response to this request, applicants have amended Fig. 1 to include the legend –**Prior Art**-- as suggested by the Examiner. No new matter has been added by this change.

The Examiner next rejected claims 1-3 and 5-11 under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art Figure 1 in view of Pruijmboom et al. (U.S. Patent Application Pub. No. 2002/0030244 A1) and Wu (U.S. Patent No. 5,998,277), since the Examiner stated that Figure 1 teaches an integrated circuit having a plurality of circuits **10** and **30** formed on a common substrate **15** and circuitry formed on predetermined portions of the common substrate. However, the Examiner continued, Figure 1 fails to teach embedded regions buried in the common substrate and isolation regions. The Examiner then stated that Pruijmboom et al. teaches embedded regions **27** buried in the common substrate **10**; and boron and phosphorus ions, while Wu teaches isolation regions **14**, where predetermined locations of a common substrate **2** are masked.

With regard to claims 2 and 7, the Examiner stated that Pruijmboom et al. teaches a common substrate **10** having low doping P- and a first predetermined resistance; circuitry formed on predetermined portions of the common substrate; embedded regions of the common substrate that are implanted with ions such that the embedded regions have a resistance that is lower than the first predetermined resistance, the embedded regions being substantially aligned with the circuitry and buried in the common substrate, respectively. Also with regard to claims 1 and 2, concerning the currents being injected into the common substrate, the Examiner stated that claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. With regard to claims 2 and 8, and also with regard to claims 1 and 7 and 9, the Examiner continued that Pruijmboom et al. teaches a common substrate including an epitaxial layer **12** and an underlying substrate layer **10**.

Since Figure 1, Pruijmboom et al. and Wu are from the same field of endeavor (integrated circuits), the Examiner concluded that the purpose disclosed by Wu would have been recognized in the pertinent art of Figure 1 and Pruijmboom et al., and that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify forming the integrated circuit of Admitted Prior Art Figure 1 by incorporating the embedded regions of Pruijmboom et al. and the isolation region of Wu to recover implant-induced damage.

Claim 4 was next rejected under 35 U.S.C. 103(a) as being unpatentable over Figure 1, Pruijmboom et al. and Wu, as applied to claims 1-3 and 5-11 above, and further in view of Rumennik et al. (U.S. Patent Application Pub. No. 2002/0050613 A1). However, the Examiner asserted that Figure 1, Pruijmboom et al. and Wu fail to teach embedded regions formed in a checkerboard pattern, whereas Rumennik et al. teaches embedded regions formed in a checkerboard pattern. The Examiner then stated that Figure 1, Pruijmboom et al. Wu and Rumennik et al. are from the same field of endeavor, (integrated circuits), so that the purpose disclosed by Rumennik et al. would have been recognized in the pertinent art of Figure 1, Pruijmboom et al. and Wu. Therefore the Examiner concluded that it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify forming the integrated circuit of Admitted Prior Art Figure 1, the embedded regions of Pruijmboom et al. and the isolation region of Wu with the checkerboard pattern embedded regions of Rumennik et al. to take advantage of multi-dimensional depletions.

Applicants respectfully disagree with the Examiner's rejections of claims 1-11 under 35 U.S.C. 103(a) for the reasons to be set forth hereinbelow. Reexamination and reconsideration are requested.

The Examiner has also cited certain prior art as pertinent to applicants' disclosure, but has not applied these references to the claimed invention. After reviewing the cited documents, applicants believe that no further response is required.

Turning now to the rejection of claims 1-11 under 35 U.S.C. 103(a), applicants first wish to point out that the second step of claim 1, as amended in the

Preliminary Amendment dated 01 February 2002, recites: "irradiating said common substrate with said high energy ions such that said high energy ions have an energy level sufficient to implant said high energy ions in embedded regions of said common substrate that have a lower resistance than said common substrate and that are substantially aligned with unmasked portions of said common substrate that are substantially aligned with said circuits so that said isolation regions having a higher resistance than said common substrate are formed in said common substrate between said embedded regions and said embedded regions are buried in said common substrate so that currents injected into said common substrate by said circuits preferentially flow to a ground potential rather than through said isolation region." Similar recitations may be found in the other independent claims of the present invention.

Pruijmboom et al., by contrast, recites on page 3, paragraphs [0025] and [0026]: "A mask, not shown, is provided on a lightly doped P type (P-) monocrystalline semiconductor substrate **10** to expose regions of the substrate to implantation of a high dose of arsenic (about 5E15/cm^2), or other N-type impurity such as P or Sb, to form buried N regions **11** having a high N-type concentration in the exposed regions of the substrate **10**. ... A second mask, not shown, is provided on the wafer **10** to expose additional regions of the wafer to implantation with a medium dose of boron (about 4E13/cm^2) to form buried P regions **27** having a conventional medium P type concentration in the exposed regions. The buried P regions **27** will form part of an isolation structure which will isolate the completed LPNP from adjacent devices."

Additionally, on page 4, paragraph [0035], it is stated that: "The mask **37** also exposes the deep N regions **23** (only) of the LPNP. An Implant of arsenic is made through the exposed areas of mask **37** which forms the external S/D regions of the NOMS transistors. The arsenic implant through mask **37** also forms the external heavily doped (N+) base active region **24**, which is located above the deep N type region **23**, in order to provide a low resistance path to buried N region **11** and reduce collector series resistance."

The present invention, by contrast, recites the formation of embedded regions in the common substrate having lower resistance than the common substrate, and that these regions drain currents injected into the common substrate from the circuits preferentially to a ground potential rather than through an isolation region between the embedded regions. As seen, Pruijmboom et al. teaches the formation of a low resistance pathway between the embedded region and the circuits formed on the surface thereof "in order to provide a low resistance path to buried N region **11** and reduce collector series resistance." Clearly then, Pruijmboom et al. teaches away from the integrated circuit of the present claimed invention, since if the low resistance pathway of Pruijmboom et al. were introduced into the common substrate of the present invention above the embedded regions, the collectors of the lateral bipolar transistors thereof would effectively be grounded and the transistors would no longer function.

Moreover, the embedded regions of Pruijmboom et al. are formed on the surface of a substrate by an ion irradiation procedure and subsequently buried by a surface coating procedure, as opposed to the process of the present invention which recites ion implantation such that embedded regions are formed beneath the surface of the chosen substrate, said regions having lower resistance than the remainder of the substrate starting material. Pruijmboom et al. therefore teaches away from the process of forming the integrated circuit of the present, as well as away from the product by process thereof.

For these reasons, applicants respectfully believe that the Pruijmboom et al. reference teaches away from the subject claimed invention, and has been improperly combined with the references identified by the Examiner in the rejection of all pending claims under 35 U.S.C. 103(a). The Examiner has therefore failed to make a *prima facie* case for an obviousness-type rejection.

As a result, applicants believe that claims 1-11, are in condition for allowance or appeal, the former action by the Examiner at an early date being earnestly solicited. Reexamination and reconsideration are respectfully requested.

Respectfully submitted,

Date: April 13, 2004

Signature of Attorney

Reg. No. 30,459
Phone (970) 377-6363

Samuel M. Freund
Cochran Freund & Young LLC
3555 Stanford Road, Suite 230
Fort Collins, Colorado 80525